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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,383	TRIVEDI ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-87* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-87 are rejected under 35 U.S.C. 102(e) as being anticipated by Dowling, U.S. Patent Number 6,363,475 (herein referred to as Dowling).

4. Referring to claims 1, 28, and 55 Dowling has taught a method for dispatching instructions executed by at least one functional unit of a data processor, each one of the instructions having a corresponding priority number, in a computer system having at least one host processor and host memory, the method comprising:

receiving a next instruction (Dowling abstract, figure 5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 18);

examining a current instruction group to determine if the current instruction group is completed (Dowling abstract, figure 5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 18);

adding the next instruction to the current instruction group if the current instruction group is not completed (Dowling abstract, figure 5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36); and

dispatching the current instruction group if the current instruction group is completed (Dowling column 14 lines 3-23).

5. Referring to claims 2, 29, and 56 Dowling has taught the method of claim 1, wherein if the current instruction group is completed, the method further comprises:

starting a new instruction group; and

adding the next instruction to the new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

6. Referring to claims 3, 30, and 57 Dowling has taught the method of claim 1, further composing:

examining the next instruction to determine if the corresponding priority number of the next instruction is equal to or lower than the corresponding priority number of a current instruction of the current instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

adding the next instruction to the current instruction group if the corresponding priority number of the next instruction is higher than the corresponding priority number of the current instruction of the current instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23); and

dispatching the current instruction group if the corresponding priority number of the next instruction is equal to or lower than the corresponding priority number of the current instruction of the current instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

7. Referring to claims 4, 31, and 58 Dowling has taught the method of claim 3, wherein if the corresponding priority number of the next instruction is higher than the corresponding priority number of the current instruction of the current instruction group, the method further comprises:

examining the next instruction to determine if the next instruction is required to be in a new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

wherein if the next instruction is required to be in a new instruction group:

adding a no-operation (NOOP) instruction to the current instruction group (Dowling column 7 lines 24-39);

dispatching the current instruction group;

starting a new instruction group; and

adding the next instruction to the new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

8. Referring to claims 5, 32, and 59 Dowling has taught the method of claim 3, wherein if the corresponding priority number of the next instruction is higher than the corresponding priority number of the current instruction of the current instruction group, the method further comprises:

examining the current instruction group to determine if the current instruction group contains a predetermined number of instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

wherein if the current instruction group contains the predetermined number of instructions:

dispatching the current instruction group;

starting a new instruction group; and

adding the next instruction to the new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

9. Referring to claims 6, 33, and 60 Dowling has taught the method of claim 1, further comprising:

examining the current instruction group to determine if the current instruction group contains a predetermined number of instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23); and

dispatching the current instruction group if the current instruction group contains the predetermined number of instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

10. Referring to claims 7, 34, and 61 Dowling has taught the method of claim 1, wherein all instructions in the current instruction group are dispatched in the same clock cycle (Dowling column 3 lines 61-63).

11. Referring to claims 8, 35, and 62 Dowling has taught the method of claim 1, further comprising:

examining the next instruction to determine latency required by the next instruction;

calculating delay cycles based on the latency; and

suspending the dispatching for a period of time corresponding to the delay cycles (Dowling column 12 lines 21-40).

12. Referring to claims 9, 36, and 63 Dowling has taught the method of claim 8, further comprising inserting an additional delay cycle during the suspension (Dowling column 12 lines 21-40).

13. Referring to claims 10, 37, and 64 Dowling has taught the method of claim 1, further comprising:

examining the next instruction to determine if the next instruction contains an illegal operation code (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23); and

issuing an error message through an interrupt mechanism, if the next instruction contains an illegal operation code (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

14. Referring to claims 11, 38, and 65 Dowling has taught the method of claim 1, wherein if the next instruction is a non-branch instruction, the method further comprises:

examining the next instruction to determine if source resources required by the next instruction are in-use (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26); and

stalling instruction dispatching if the source resources required by the next instruction are in-use (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

15. Referring to claims 12, 39, and 66 Dowling has taught the method of claim 11, wherein the source resources are defined by source operand registers required by the next instruction (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

16. Referring to claims 13, 40, and 67 Dowling has taught the method of claim 1, wherein if the next instruction is a non-branch instruction, the method further comprises:

examining the next instruction to determine if destination resources required by the next instruction are in-use (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26); and

stalling instruction dispatching if the destination resources required by the next instruction are in-use (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

17. Referring to claims 14, 41, and 68 Dowling has taught the method of claim 13, wherein the destination resources are defined by target destination registers required by the next instruction (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

18. Referring to claims 15, 42, and 69 Dowling has taught the method of claim 1, wherein if the next instruction is a branch instruction, the method further comprises:

examining resources required by the branch instruction to determine if the resources are used or altered by a non-branch instruction (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26, figure 7); and

wherein if the resources are used or altered by a non-branch instruction, suspending the dispatching the next instruction until the resources are available (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

19. Referring to claims 16, 43, and 70 Dowling has taught the method of claim 15, further comprising inserting an additional delay cycle during the suspension (Dowling abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

20. Referring to claims 17, 44, and 71 Dowling has taught the method of claim 5, wherein the predetermined number of instructions comprises four instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

21. Referring to claims 18, 45, and 72 Dowling has taught the method of claim 6, wherein the predetermined number of instructions comprises four instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

22. Referring to claims 19, 46, and 73 Dowling has taught the method of claim 3, further comprising accessing a database to determine the corresponding priority number of the next instruction (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

23. Referring to claims 20, 47, and 74 Dowling has taught the method of claim 8, further comprising accessing a database to determine the latency required by the next instruction (Dowling column 12 lines 21-40).

24. Referring to claims 21, 48, and 75 Dowling has taught the method of claim 1, wherein the data processor is integrated in a system core logic chip that functions as a bridge between the host processor and the host memory, and other components of the computer system, the system core logic chip having a host interface coupled to the host processor and a memory interface coupled to the host memory (Dowling abstract, figures 2, 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

25. Referring to claims 22, 49, and 76 Dowling has taught the method of claim 1, wherein the data processor may be a stand-alone processor, or the data processor may be a co-processor to the host processor (Dowling abstract, figures 2, 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

26. Referring to claims 23, 50, and 77 Dowling has taught the method of claim 1, wherein the at least one functional unit comprises multiple functional units of a kind (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

27. Referring to claims 24, 51, and 78 Dowling has taught the method of claim 23, further comprising:

examining the next instruction to determine if there is a corresponding functional unit that executes the next instruction available (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

adding the next instruction to the current instruction group if the corresponding functional unit is available (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23); and

dispatching the current instruction group if the corresponding functional unit is not available (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

28. Referring to claims 25, 52, and 79 Dowling has taught the method of claim 24, wherein if the corresponding functional unit that executes the next instruction is available, the method further comprises:

examining the next instruction to determine if the next instruction is required to be in a new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

wherein if the next instruction is required to be in a new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

adding a no-operation (NOOP) instruction to the current instruction group (Dowling column 7 lines 24-39);

dispatching the current instruction group;

starting a new instruction group; and

adding the next instruction to the new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

29. Referring to claims 26, 53, and 80 Dowling has taught the method of claim 24, wherein if the corresponding functional unit that executes the next instruction is available, the method further comprises:

examining the current instruction group to determine if the current instruction group contains a predetermined number of instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

wherein if the current instruction group contains the predetermined number of instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

dispatching the current instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

starting a new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23); and

adding the next instruction to the new instruction group (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

30. Referring to claims 27, 54, and 81 Dowling has taught a method of claim 26, wherein the predetermined number of instructions comprises four instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

31. Referring to claim 82 Dowling has taught an apparatus for dispatching instructions executed by at least one functional unit of a data processor, the apparatus comprising:

an instruction cache memory for receiving instructions from an input and output (1/0) interface (Dowling abstract, figures 2 and 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23);

an instruction decoder coupled to construct an instruction group based on the priorities of the instructions (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23); and

a dispatch controller coupled to dispatch the instruction group to an appropriate functional unit (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

32. Referring to claim 83 Dowling has taught the apparatus of claim 82, further comprising:

at least one instruction registers coupled to store the instructions being grouped; and

at least one instruction buffers coupled to store instructions when the instruction fetching is stalled (Dowling abstract, figures 4-5, column 3 line 54-column 4 line 6, column 12 line 41-column 13 line 36, column 14 lines 3-23).

33. Referring to claim 84 Dowling has taught the apparatus of claim 82, further comprising a branch decoder coupled to detect a branch condition and to generate the address for the next instruction being fetched (Dowling figure 7, abstract, column 3 lines 13-30, column 7 lines 3-23).

34. Referring to claim 85 Dowling has taught the apparatus of claim 84, further comprising a program counter coupled to receive commands from the branch decoder to fetch the next

instruction at the address (Dowling figure 7, abstract, column 3 lines 13-30, column 7 lines 3-23).

35. Referring to claim 86 Dowling has taught the apparatus of claim 83, wherein the instruction decoder retrieves the instructions from the at least one instruction registers or from the at least one instruction buffers after the instruction stalling cycles (Dowling column 12 lines 21-40, abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

36. Referring to claim 87 Dowling has taught the apparatus of claim 82, wherein the instruction decoder stalls the instruction fetching based on the latency of the instruction being executed (Dowling column 12 lines 21-40, abstract column 8 lines 40-58, column 10 line 63-column 11 line 26).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kahle et al., U.S. Patent Number 5,978,896, has taught a system for increased dispatching for a superscalar machine.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Harkness

Examiner

2183

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